CLAIMS:

What is claimed is:

1. A method in a data processing system for processing a parity error, the method comprising:

responsive to an occurrence of a parity error, storing processor information to form stored processor information;

determining whether the parity error is a recoverable parity error using the stored processor information; and

responsive to the parity error being a recoverable parity error, performing a recovery action.

2. The method of claim 1, wherein the performing step comprising:

if an error type for the parity error is one of a level one data cache error or a level one cache tag error, incrementing an error count associated with the error type and invalidating the level one data cache; and

if the error count associated with the error type is greater than a threshold, disabling the failing portion of the level one data cache or data cache tag.

3. The method of claim 1, wherein the performing step comprises:

if an error type is a translation lookaside buffer error, incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer.

4. The method of claim 3, wherein the performing step further comprises:

if the translation lookaside buffer error count is greater than a threshold, disabling the failing portion of the translation lookaside buffer.

5. The method of claim 1, wherein the performing step comprises:

if an error type is an effective to real address translation error, incrementing and error count and invalidating selected entries within a translation lookaside buffer.

6. The method of claim 5, wherein the selected entries are every fourth entry within the translation lookaside buffer.

7. The method of claim 5, wherein the performing step further comprises:

if the effective to real address translation error count is greater than a threshold, disabling the failing portion of the effective to real address translation unit.

8. The method of claim 1, wherein the stored processor information includes at least one error state.

9. The method of claim 1 further comprising:

if the parity error is a non-recoverable parity error generating an indication of the non-recoverable interrupt error.

10. A method in a data processing system for error recovery, the method comprising:

saving processor information from a processor in response to detecting an occurrence of an error associated with the processor;

determining whether the error is a recoverable error; and

responsive to the error being a recoverable error, performing a selected action.

11. The method of claim 10, wherein the processor information includes the recoverable state of the processor at the time of the interrupt and wherein the determining step comprises:

determining whether the interrupt is recoverable.

12. The method of claim 10, wherein stored processor information includes at least one error state.

13. The method of claim 10, wherein the error is a parity error.

14. The method of claim 10, wherein the performing step comprising:

if an error type for the error is one of a level one data cache error or a level one cache tag error, incrementing an error count and invalidating the level one data cache; and

if the error count is greater than a threshold, disabling the failing portion of the level one data cache.

15. The method of claim 10, wherein the performing step comprises:

if an error type is a translation lookaside buffer error, incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer.

16. The method of claim 13 wherein the performing step further comprises:

if the error count is greater than a threshold, disabling the failing portion of the translation lookaside buffer.

17. The method of claim 10, wherein the performing step comprises:

if an error type is an effective to real address translation error, incrementing an effective to real address translation error count and invalidating selected entries within a translation lookaside buffer.

18. The method of claim 17, wherein the selected entries are every fourth entry within the translation lookaside buffer.

19. The method of claim 17, wherein the performing step further comprises:

if the error count is greater than a threshold, disabling the failing portion of the effective to real address translation unit.

20. A data processing system comprising:

a bus system;

a communications unit connected to the bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit includes hardware logic to save processor information to form stored processor information in response to the detection of a parity error; branch to the machine check interrupt vector, a runtime system firmware executes by the processing unit at the interrupt vector to determine whether the parity error is a recoverable parity error using the stored processor information; and perform a recovery action in response to the parity error being a recoverable parity error.

21. The data processing system of claim 20, wherein the bus system is a single bus.

22. The data processing system of claim 20, wherein the bus system includes a primary bus and a secondary bus.

23. The data processing system of claim 20, wherein the processing unit includes a plurality of processors.

24. The data processing system of claim 20, wherein the communications unit is one of a modem and Ethernet adapter.

25. A data processing system comprising:

a bus system;

a communications unit connected to the bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit includes hardware logic to save processor information from a processor in response to detecting an occurrence of an error associated with the processor; branch to the machine check interrupt vector, a runtime system firmware executing on the processing unit at the interrupt vector to determine whether the error is a recoverable error; and perform a selected action in response to the error being a recoverable error.

26. The data processing system of claim 25, wherein the bus system is a single bus.

27. The data processing system of claim 25, wherein the bus system includes a primary bus and a secondary bus.

28. The data processing system of claim 25, wherein the processing unit includes a plurality of processors.

29. The data processing system of claim 25, wherein the communications unit is one of a modem and Ethernet adapter.

30. A data processing system for processing a parity error, the data processing system comprising:

storing means, responsive to an occurrence of a parity error, for storing processor information to form stored processor information;

determining means for determining whether the parity error is a recoverable parity error using the stored processor information; and

performing means, responsive to the parity error being a recoverable parity error, for performing a recovery action.

31. The data processing system of claim 30, wherein the performing means comprises:

incrementing means, if an error type for the parity error is one of a level one data cache error or a level one cache tag error, for incrementing an error count associated with the error type and invalidating the level one data cache; and

disabling means, if the error count is greater than a threshold, for disabling the failing portion of the level one data cache.

32. The data processing system of claim 30, wherein the performing means comprises:

means for incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer if an error type is a translation lookaside buffer error.

33. The data processing system of claim 32, wherein the performing means further comprises:

means for disabling the failing portion of the translation lookaside buffer if the error count is greater than a threshold.

34. The data processing system of claim 30, wherein the performing means comprises:

means for incrementing an effective to real address translation error count and invalidating selected entries within a translation lookaside buffer if an error type is an effective to real address translation error.

35. The data processing system of claim 34, wherein the selected entries are every fourth entry within the translation lookaside buffer.

36. The data processing system of claim 34, wherein the performing means further comprises:

means for disabling the failing portion of the effective to real address translation unit if the error count is greater than a threshold.

37. The data processing system of claim 30, wherein the stored processor information includes at least one error state.

38. The data processing system of claim 30 further comprising:

generating means for generating an indication of the non-recoverable interrupt if the parity error is a non-recoverable parity error.

39. A data processing system for error recovery, the data processing system comprising:

saving means for saving processor information from a processor in response to detecting an occurrence of an error associated with the processor;

determining means for determining whether the error is a recoverable error;

performing means, responsive to the error being a recoverable error, for performing a selected action.

40. The data processing system of claim 39, wherein the processor information includes the recoverable state of the processor at the time of the interrupt and wherein the determining means comprises:

means for determining whether the interrupt is recoverable.

41. The data processing system of claim 39, wherein stored processor information includes at least one error state.

42. The data processing system of claim 39, wherein the error is a parity error.

43. The data processing system of claim 39, wherein the performing step comprising:

incrementing means, if an error type for the error is one of a level one data cache error or a level one cache tag error, for incrementing a D-cache or D-cache tag error count and invalidating the level one data cache; and

disabling means, if the error count is greater than a threshold, for disabling the failing portion of the level one data cache.

44. The data processing system of claim 39, wherein the performing means comprises:

means for incrementing a translation lookaside buffer error count and invalidating all entries in a translation lookaside buffer if an error type is a translation lookaside buffer error.

45. The data processing system of claim 44, wherein the performing means further comprises:

means for disabling the failing portion of the translation lookaside buffer if the error count is greater than a threshold.

46. The data processing system of claim 39, wherein the performing means comprises:

means for incrementing a effective to real address translation error count and invalidating selected entries within a translation lookaside buffer if an error type is an effective to real address translation error.

47. The data processing system of claim 46, wherein the selected entries are every fourth entry within the translation lookaside buffer.

48. The data processing system of claim 46, wherein the performing means further comprises:

means for disabling the failing portion of the effective to real address translation unit if the error count is greater than a threshold.

49. A computer program product in a computer readable medium for processing a parity error, the computer program product comprising:

first instructions for determining whether the parity error is a recoverable parity error using the stored processor information; and

second instructions, responsive to the parity error being a recoverable parity error, for performing a recovery action.

50. A computer program product in a computer readable medium for error recovery, the computer program product comprising:

first instructions for determining whether the error is a recoverable error; and

second instructions, responsive to the error being a recoverable error, for performing a selected action.